REMARKS/ARGUMENTS

Claims 8-13 are pending in this application. By this Amendment, Applicant amends Claim 8 and cancels Claims 14-21.

Applicant has canceled Claims 14-21 because these claims are directed to a non-elected species and are not dependent upon a generic claim. Non-elected Claim 13 is dependent upon generic Claim 8. Therefore, Applicant respectfully requests that the Examiner rejoin and allow non-elected Claim 13 when Claim 8 is allowed.

Claims 8-12 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Nakatani et al. (U.S. 6,625,037) in view of Sugaya et al. (U.S. 6,931,725). Applicant notes that, although the Examiner indicated that the rejection of Claims 8-12 was over Nakatani et al. in view of Sugaya et al., the description of this rejection clearly sets forth a rejection of Claims 8-12 over Sugaya et al. in view of Nakatani et al. Applicant respectfully traverses the rejection of Claims 8-12.

Claim 8 has been amended to recite:

> A process for producing a component-embedded substrate, comprising the steps of:
>
> connecting and fixing a first electronic component to a first electrode pattern on a first supporting layer with a conductive bonding material;
>
> **press-bonding a second supporting layer including a second electrode pattern onto the electronic component-fixed surface of the first supporting layer with a first prepreg therebetween to perform transfer**;
>
> separating the first supporting layer and the second supporting layer from the first prepreg such that the first and second electrode patterns are disposed on a front surface and a back surface of the first prepreg;
>
> curing the first prepreg before or after the step of separating the first supporting layer and the second supporting layer from the first prepreg;
>
> **connecting and fixing a second electronic component onto a back surface of the second electrode pattern with a conductive bonding material after the step of curing the first prepreg**;
>
> press-bonding a third supporting layer including a third electrode

pattern onto a second electronic component-fixed surface with a second prepreg therebetween to perform transfer;

separating the third supporting layer from the second prepreg; and

curing the second prepreg before or after the step of separating the third supporting layer from the second prepreg, wherein the prepregs and the electrode patterns are sequentially laminated. (emphasis added)

With the unique combination and arrangement of features and method steps recited in Applicant's Claim 8, including the steps of "connecting and fixing a second electronic component onto a back surface of the second electrode pattern with a conductive bonding material after the step of curing the first prepreg" and "press-bonding a second supporting layer including a second electrode pattern onto the electronic component-fixed surface of the first supporting layer with a first prepreg therebetween to perform transfer," Applicant has been able to provide a process for producing a component-embedded substrate having low connection resistance between laminated electrode patterns (see, for example, paragraph [0007] of the Substitute Specification).

The Examiner alleged that Sugaya et al. teaches all of the features and method steps recited in Claim 8, except for "the manner used to attach a second electronic component." The Examiner further alleged that Nakatani et al. teaches a method including the steps of connecting and fixing a second electronic component onto a back surface of a second electrode pattern, press-bonding a third supporting layer including a third electrode pattern, and separating the third supporting layer from the second prepreg. Thus, the Examiner concluded that it would have been obvious "to provide [the] Sugaya et al. reference with the second component attached, pressed and heated as taught by Nakatani et al. in order to allow 'the epoxy resin in the sheet to be cured, so that the circuit components and the wiring pattern and the sheet were strongly connected mechanically.'" Applicant respectfully disagrees.

Applicant's Claim 8 has been amended to recite the step of "connecting and fixing a second electronic component onto a back surface of the second electrode

pattern with a conductive bonding material **after the step of curing the first prepreg**" (emphasis added). Support for this feature is found, for example, in paragraph [0055] of the Substitute Specification.

As acknowledged by the Examiner, Sugaya et al. teaches a process for producing a component-embedded substrate which includes **only a single prepreg**. Sugaya et al. fails to teach or suggest any second electrode pattern, any method step for connecting a second electronic component to a back surface of a second electrode pattern, or any step for involving a second prepreg. In fact, Sugaya et al. fails to teach or suggest anything at all about a second prepreg.

Contrary to the Examiner's allegations, col. 13, line 37 to col. 14, line 18 of Nakatani et al. disclose:

> In parallel to the processes of FIGS. 6(a) and 6(b), a plurality of sheets in which the wiring pattern 606 and the circuit components are buried are formed in the same manner as those shown in FIGS. 6(a) and 6(b) (refer to FIGS. 6(c) and 6(d)). The wiring pattern 606 and the circuit components are different from layer to layer in accordance with the design.
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> In parallel to the processes of FIGS. 6(a) and 6(b), as shown in FIG. 6(e), a wiring pattern 607 is formed on the release film 603.
>
> Thereafter, as shown in FIG. 6(f), the sheet of FIG. 6(d) is positioned and superimposed on the sheet of FIG. 6(b). Then, the release film 603 of FIG. 6(e) is superimposed on a principal plane of the sheet of FIG. 6(d) on which the wiring pattern 606 is not formed so that the wiring pattern 607 on the release film 603 faces inwards
>
> Thereafter, **the sheets and the release film 603 are positioned and attached to each other in the process shown in FIG. 6(f), pressed and heated, so that a sheet having a multilayered structure can be formed, as shown in FIG. 6(g).** The heating is performed at a temperature equal to or higher than a temperature at which the thermosetting resin in the mixture 600 and the conductive resin composition 601 is cured (e.g., 150° C to 260° C). The mixture 600 serves as an insulating substrate 608, and the conductive resin composition 601 serves as an inner via 609. This process allows the active component 604, the passive component 605, the wiring pattern 606 and 607 and the insulating substrate 608 to strongly adhere mechanically. The inner via 609 electrically connects the wiring patterns 606 and 607. (emphasis

added)

As disclosed above, the sheet shown in Figs. 6(a) and 6(b) of Nakatani et al. and the sheet shown in Figs. 6(c) and 6(d) of Nakatani et al. are assembled in parallel to one another (i.e., concurrently with one another). Once the two sheets are assembled, the sheets and a release film 603 are positioned and attached to each other, and then are pressed and heated so as to cure both of the first and second prepregs 600. In other words, in Nakatani et al., the step of connecting and fixing a second electronic component is performed **before** the step of curing of the first prepreg 600. Nakatani et al. neither teaches nor suggests that the step of connecting and fixing a second electronic component could or should be performed **after** the step of curing of the first prepreg 600. Thus, Nakatani et al. certainly fails to teach or suggest the step of "connecting and fixing a second electronic component onto a back surface of the second electrode pattern with a conductive bonding material **after** the step of curing the first prepreg" (emphasis added) as recited in Applicant's Claim 8.

Even assuming *arguendo* that Nakatani et al. taught or suggested that the step of connecting and fixing a second electronic component could be performed after the step of curing of the first prepreg, Nakatani et al. still fails to cure the deficiencies of Sugaya et al. Particularly, as shown in Figs. 6(a) through 6(g) of Nakatani et al., the first prepreg 600 of Nakatani et al. (the lower sheet shown in Fig. 6(f)) includes only a first electrode pattern embedded in a lower surface of the first prepreg 600. The first prepreg 600 of Nakatani et al. does not include any second electrode pattern. Thus, Nakatani et al. clearly fails to teach or suggest the step of "press-bonding a second supporting layer including a second electrode pattern onto the electronic component-fixed surface of the first supporting layer with a first prepreg therebetween to perform transfer" as recited in Applicant's Claim 8.

Since Nakatani et al. fails to teach or suggest any second electrode pattern, Nakatani et al. certainly fails to teach or suggest the step of "connecting and fixing a

second electronic component onto a back surface of the second electrode pattern with a conductive bonding material after the step of curing the first prepreg" as recited in Applicant's Claim 8. Instead of being connected and fixed to a second electrode pattern of a first prepreg, the second electronic component 604 of Nakatani et al. is connected and fixed to a first electrode pattern embedded in the second prepreg 600 (the upper sheet shown in Fig. 6(f) of Nakatani et al.).

Accordingly, Applicant respectfully submits that Sugaya et al. and Nakatani et al., applied alone or in combination, fail to teach or suggest the unique combination and arrangement of features and method steps recited in Applicant's Claim 8.

Accordingly, Applicant respectfully requests reconsideration and withdrawal of the rejection of Claim 8 under 35 U.S.C. § 103(a) as being unpatentable over Sugaya et al. in view of Nakatani et al.

In view of the foregoing amendments and remarks, Applicant respectfully submits that Claim 8 is allowable. Claims 9-12 depend upon Claim 8, and are therefore allowable for at least the reasons that Claim 8 is allowable. In addition, Applicant respectfully requests that the Examiner rejoin and allow non-elected Claim 13.

In view of the foregoing amendments and remarks, Applicant respectfully submits that this application is in condition for allowance. Favorable consideration and prompt allowance are solicited.

To the extent necessary, Applicant petitions the Commissioner for a One-Month Extension of Time, extending to February 18, 2008 (February 17, 2008 falls on a Sunday), the period for response to the Office Action dated October 17, 2007.

The Commissioner is authorized to charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account No. 50-1353.

Respectfully submitted,

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